LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A trench-type power MOSFET having a vertical invertible channel composed of N type conductivity material and disposed between a source region and a drain region; a gate oxide and gate contact thereon extending along the length of said invertible channel and operable to invert the conductivity type of said invertible channel; said gate contact containing a P type conductivity material; said vertical invertible channel material having a constant concentration along its full length; a source contact connected to at least said source region; and a drain contact made of metal and connected to a bottom surface of said drain region.

Claim 2 (Canceled).

3. (Previously Presented) The power MOSFET of claim 1 wherein said invertible channel material is epitaxially deposited silicon.

4. (Currently Amended) A power MOSFET comprising, in combination, a P type substrate; an epitaxially deposited N type layer deposited atop said substrate and having a substantially constant concentration; a plurality of spaced trenches having vertical walls extending through said epitaxial layer; a thin gate oxide on said vertical walls and conductive P type polysilicon deposited into said trenches to define a polysilicon gate; a P type source region formed adjacent the walls of each of said trenches and diffused into the top of said epitaxial layer; a source contact connected to at least said source regions; a drain contact made of metal and connected to a bottom surface of said substrate; whereby said MOSFET has a reduced on resistance.

5. (Original) The MOSFET of claim 4 wherein said source contact is connected to said source region only, whereby said MOSFET is bidirectional.

6. (Currently Amended) The MOSFET of claim 4, further comprising a plurality of spaced notches extending through said source regions and exposing said epitaxial deposited layer, wherein said source contact extends through said plurality of notches and is connected to said epitaxially deposited layer.

Claim 7 (Canceled).

8. (Currently Amended) The MOSFET of claim [[7]] 4 wherein said epitaxial region has a resistivity of about 0.17 ohm cm and a thickness of about 2.5 μm.

9. (Currently Amended) A power MOSFET having reduced on resistance comprising, in combination; a P type conductivity substrate; an epitaxially deposited N type conductivity layer deposited atop said P type substrate to form an epitaxial layer having a substantially constant concentration throughout its volume; a plurality of spaced trenches having vertical walls extending through said epitaxial layer; a thin gate oxide on said vertical walls and conductive polysilicon with a P type conductivity deposited into said trenches to define a polysilicon gate; a P type concentration source region formed adjacent the walls of each of said trenches and diffused into the top of said epitaxial layer; a source contact connected to at least said source regions; and a drain contact made of metal and connected to a bottom surface of said substrate.

10. (Currently Amended) The MOSFET of claim 9, further comprising a plurality of spaced notches extending through said source regions and exposing said epitaxial deposited layer, wherein said source contact extends through said plurality of notches and is connected to said epitaxially deposited layer.

11. (Previously Presented) The MOSFET of claim 10 wherein said epitaxial layer has a resistivity of about 0.17 ohm cm and a thickness of about 2.5 μm.

12. (Previously Presented) The MOSFET of claim 9 wherein said substrate is a P^+ substrate having a resistivity of less than about 0.005 ohm cm.

13. (Previously Presented) The MOSFET of claim 10 wherein said substrate is a P^+ substrate having a resistivity of less than about 0.005 ohm cm.

Claims 14-19 (Canceled).

20. (Previously Presented) A trench-type power MOSFET according to claim 1, further having highly doped contact regions at a top portion of said vertical invertible channel.

21. (Previously Presented) A power MOSFET according to claim 4, further comprising highly doped contact regions in said epitaxial layer.

22. (Previously Presented) A power MOSFET having reduced on resistance according to claim 9, further comprising highly doped contact regions in said epitaxial layer.